A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed including Ti/TiN salicided contact surface regions thereto. A thin layer of silicon oxide and a thick layer of photoresist are deposited. The layer of photoresist is polished, stopping on a top layer of BN of the gate electrode. The exposed layer of BN is removed. A thick layer of Ti/TiN is next deposited and annealed, forming $TiSi_x$ after which unreacted Ti/TiN is removed. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the layer of BN can be replaced with a layer of silicon nitride.

By using a layer of BN as a top layer over the gate electrode, as specified in claim 13 of the instant invention, this layer provides an excellent stop layer for polishing the thick layer of photoresist. The layer of boron nitride serves as a CMP stop layer since the polishing rate of the photoresist is higher than the polishing rate of the layer of boron nitride, providing a method of exposing the surface of the gate electrode for further salicidation of that surface.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 13-24 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,180,501) in view of McAnally (U.S. Patent 6,136,700) is respectfully requested based on the following.

Pey et al. provides for the creation of a double polysilicon gate structure, the instant invention provides for a method of fabricating field effect transistors having low sheet resistance gate electrodes.

Specifically, Pey et al. provide for:

- Fig. 4, a gate electrode having a silicon nitride cap 22 and silicon nitride gate spacers 20
- Fig. 6, a layer 26 of Ti/TiN is deposited for purposes of salicidation
- Fig. 8, after salicidation (Fig. 7) a layer 32 of TEOS is deposited and polished (Fig. 9)
- Fig. 10, and contact opening 36 is created in the layer of TEOS for access to the top of gate electrode
- Figs. 11 through 12c, a second poly gate is formed as an extension of the first poly gate 12 (40, a stud shaped additional gate in Fig. 12a; 42, a T-shaped additional gate in Fig. 12b; and 43, a relatively short stud shaped additional gate

in Fig. 12c); these extended gate electrodes are show in Fig. 13a (the extended stud shape) and 13b (the T-shaped) after layer 44 of photoresist has been removed from the surface

- Fig. 13c through 15b, a thin layer 46 of Ti/Tin or Cobalt/Titanium is deposited and salicided over the extended gate structure, forming salicided layer 48, in Fig. 15a for the stud shaped extended gate structure, in Fig. 15b for the T-shaped extended gate structure and in Fig. 14c for the relatively short stud shaped extended gate structure.

The instant invention provides for, essentially following claim 13 of the instant invention:

- Figs. 8-9, providing a gate structure with salicided source/drain contact surfaces over a semiconductor substrate, a layer 17 of BN is the top layer of the gate electrode
- Fig. 9, depositing a liner layer 31 of silicon dioxide
- Fig. 9, depositing a layer 33 of photoresist over the liner layer 31
- Fig. 10, polishing the surface of the layer of photoresist down to the surface of the layer 17 of BN, using the layer 17 of BN as a stop for the process of polishing
- Fig. 11, removing the layer 17 of BN from above the one gate electrode, exposing the surface of the gate electrode

- Fig. 12, depositing a thick layer 35 of Ti/TiN as salicide material over the surface of the polished layer of dielectric including the exposed surface of the gate electrode
- Fig. 12 applying a low temperature anneal, annealing the deposited thick layer 35 of salicide material, saliciding the top surface of the gate electrode
- Fig. 13, applying a selective etch to remove un-salicided material, and
- Fig. 13, performing a high temperature anneal.

The difference between the instant invention and the invention provided by Pey et al. can best be illustrated by highlighting the steps that are provided by Pey et al. that are not part of the instant invention, as follows.

The instant invention does not provide the following steps that are provided by Pey et al.:

- providing a gate electrode having a silicon nitride cap 10 (not highlighted but initially highlighted as layer 10, Fig. 1 of Pet et al.) and silicon nitride gate spacers 20
- depositing a layer 32 of TEOS (Fig. 8, Pet et al.), the TEOS is polished (Fig. 9, Pet et al.)
- creating a contact opening 36, Fig. 10 Pet et al., through a layer 34 of TEOS for access to the top of gate electrode; the

top layer 22 if nitride is removed from the surface of the gate electrode, exposing the layer 12 of polysilicon

- depositing a layer 38, Fig. 11 of Pet et al., of polysilicon for the formation of extended gate electrodes
- patterning and etching the deposited layer 38, fig. 11 pf Pet et al., of polysilicon, forming a (extended plug shaped or T-shaped or relatively short stud shaped) second poly gate as an extension of the first poly gate
- saliciding the surface of the second poly gate.

Inversely, the instant invention provides for the following steps that are not provided by Pey et al.:

- providing the gate electrode with a top layer of BN
- depositing a layer of liner oxide over a gate electrode that has been provided with salicided source/drain surfaces
- depositing a layer of dielectric, preferably comprising photoresist, over the surface of the layer of etch stop material
- polishing the surface of the layer of dielectric down to the surface of the layer of BN, using the layer of BN as a stop for the process of polishing
- removing the layer of BN material from above the one gate electrode

- depositing a thick layer of Ti/TiN over the surface of the polished layer of dielectric including the exposed surface of the gate electrode
- performing a low temperature anneal, annealing the deposited thick layer of salicide material, saliciding the top surface of the gate electrode
- by selective etch removing un-reacted Ti/Tin, and
- performing a low temperature anneal.

Layer 110, used by McAnally as a stop layer is an etch stop layer, which is not related to a polish stop layer as provided by the instant invention and as shown in the cross section of Fig. 10 of the instant invention.

The "stopping layer" (layer 110, Figs. 1B e.a.) that is used by McAnnaly and referred to by Examiner is an etch stopping layer, providing, col. 4, lines 63 e.a., a high etch selectivity ratio between insulating layer 112 and the etch stopping layer 110. This layer is therefore selected such that the layer has a silicon level greater than that required by stoichiometric proportions (Pet et al., col. 5, lines 5 e.a.).

The layer 17 of boron nitride that is used by the instant invention is used as a polishing stop layer (for CMP processes)

and must therefore have a surface hardness that contributes to serving as an polishing stop. In addition, the polishing rate of the surrounding layer 33 of filler material (such as photoresist) must be higher that the polishing rate of the layer (17 of boron nitride) that is used for a polishing etch stop for the simple reason that, without this requirement, layer 17 would be polished (away) and the polishing of the layer of filler material would continue unhindered (or: not stopped) by the layer 17 of boron nitride. In addition, and as specified in claim 13, the layer of boron nitride is removed (Fig. 11 of the instant invention) after it has served its purpose (of stop layer for the CMP processes) so that the layer 16 of polysilicon can be salicided, see Figs. 12 and 13 of the instant invention.

The key aspects of the instant invention are the use of the layer 17, Fig. 9, of BN as a cap layer for the polysilicon gate in addition to the application of a layer 31 of silicon oxide and the dielectric 33, Fig. 9, preferably comprising photoresist.

The advantages that are provided by these key aspects of the instant invention are that, since the polishing selectivity for photoresist and silicon oxide (PR/SiO_2) is larger than about 30 and the polishing selectivity for photoresist/BN (PR/BN) is

larger than about 200, the polishing process can safely stop on the layer 17 of BN, in this manner preventing the typical corrosion of a conventional process.

While applicant acknowledges the teachings of Pey et al. and McAnally et al. as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Pey et al. with McAnally et al., applicant nonetheless also asserts that there is absent within the portions of Pey et al. and McAnally et al. or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's invention as taught and claimed within amended claim 13.

In this regard, applicant claims that there is absent form the portions of Pey et al. and McAnally et al. or any combination thereof, as cited by Examiner, a teaching of enabling accessing the top surface of the layer of polysilicon that is used for the gate electrode for purposes of saliciding this layer. By providing a layer of boron nitride over the surface of the layer of polysilicon, this layer allows the effective separation of first saliciding the source/drain regions of the gate electrode (Fig. 9 of the instant invention)

and then and as a separate processing sequence (Figs. 10-13 of the instant invention) saliciding the surface of the gate electrode. For this latter salicidation, surfaces that are not to salicided, that is all surfaces other than the surface of the layer of polysilicon of the gate electrode, must be protected, a protection that is provided by layer 31 of silicon oxide and layer 33 of filler (photoresist) material. The layer 17 of boron nitride is critically important in the removal, down to the surface of the layer 17 of boron nitride, of the layer of filler (photoresist) material, a removal that is most readily affected by applying CMP to the layer of filler material. For this CMP a good end-point must be provided for obvious reasons of closeness of elements (gate spacers, gate electrode material). This good end point is provided by the layer of boron nitride. After the layer of filler material has been polished, the layer of boron nitride must be removed so that the layer of polysilicon is exposed and can be salicided as a separate processing sequence (Figs. 12, 13 of the instant invention).

It would not be obvious to combine the teachings of Pey et al. with those of McAnally et al. since there is no suggestion or motivation in the teachings of any of the patents of the present invention. Contrary to the Examiner's assertion that Pey et al. provides for a gate electrode that would suggest the

process of the instant invention, Pey et al. does not provide for a cost-effective and dependable method of first saliciding the source/drain surfaces and then saliciding the gate electrode. Pey et al. discloses forming a double-polysilicon gate structure and does not mention the formation of a single-polysilicon gate electrode with separate processing sequences for the salicidation of the source/drain surfaces and the surface of the gate electrode.

None of the applied or known references address the invention as shown in the amended claims in which a gate electrode is created, the contact surfaces of the gate electrode are salicided as separate processing step and a method is provided for the protection of the layer of gate material up to the point where this surface is salicided, thereby assuring a low contact resistance surface of the gate electrode. The invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these various references cannot be made without reference to Applicant's own invention. None of the applied references address the problem of gate electrode salicidation as provided by the instant invention and as specified in amended claim 13 and supporting claims of the instant invention. The processes of Figs. 8-13 (Claims 13-24) are both believed to be novel and

patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request Examiner Maria F. Guerrero to reconsider his rejection in view of these arguments and the amendments to the Claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 13-24 under 35 U.S.C 103(a) as being unpatentable over Pey et al. (US Patent 6,180,501) in view of McAnally (U.S. Patent 6,136,700), be withdrawn.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

SUMMARY

A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed including Ti/TiN salicided contact surface regions thereto. A thin layer of silicon oxide and a thick layer of photoresist are deposited.

The layer of photoresist is polished, stopping on a top layer of BN of the gate electrode. The exposed layer of BN is removed. A thick layer of Ti/TiN is next deposited and annealed, forming $TiSi_x$ after which unreacted Ti/TiN is removed. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the layer of BN can be replaced with a layer of silicon nitride.

It is requested that should Examiner not find the claims to be allowable that he call the undersigned Attorney at his convenience at 845-452-5863 to overcome any problems preventing allowance.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned:

"Version with markings to show changes made."

Respectfully submitted,

Stephen B. Ackerman (Reg. No 37,761)

Version with markings to show changes made

IN THE CLAIMS

13. (Twice Amended) A method of fabricating field effect transistors having low sheet resistance gate electrodes, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with at least one gate electrode created over an active surface region as said substrate as defined by regions of Shallow Trench Isolation provided in the surface of the said substrate, said at least one gate electrode having been provided with gate spacers, impurity implants of source and drain regions in addition to Lightly Doper Diffusion regions having been provided in the surface of said substrate self-aligned with said at least one gate electrode, said at least one gate electrode comprising a stack of layers of pad oxide created over the surface of said substrate, a layer of polysilicon patterned over the layer of pad oxide and a layer of boronitride patterned over the layer of polysilicon;

depositing a thin layer of salicide material over the surface of said substrate, including the surface of said gate spacers and said layer of polysilicon provided for said at least one gate electrode;

performing a first anneal, forming salicided layers comprising reacted salicide material over the surface of said source and drain implants;

first removing un-reacted salicide material from the surface of said substrate;

depositing an isolation film over the surface of said substrate, including the surface of said gate spacers and said layer of boronitride provided for said at least one gate electrode;

depositing a layer of filler material over the surface of said isolation film to a thickness such that the surface of said layer of filler material extends above the surface of said isolation film even where said isolation film overlays the surface of said at least one gate electrode;

polishing the surface of said layer of filler material and said layer of isolation film down to the surface of said layer of boronitride of said at least one gate electrode, using said layer of boronitride as a stop for said process of polishing, advantageously using a polishing rate of filler material that is larger than a polishing rate of boronitride, said layer of

boronitride providing a save stop for said polishing the surface of the layer of filler material and the layer of isolation film, thereby further preventing corrosion of the surface of said at least one gate electrode;

removing said layer of boronitride from said at least one gate electrode, exposing the surface of said layer of polysilicon forming part of said at least one gate electrode;

depositing a thick layer of salicide material over the surface of said polished layer of filler material, including the exposed surface of said layer of polysilicon;

performing a second anneal of said deposited thick layer of salicide material, a layer of reacted salicide material overlying said layer of polysilicon of said at least one gate electrode;

second removing un-reacted salicide material from the surface of said layer of dielectric;

performing a third anneal, reducing the sheet resistance of said reacted salicide material overlying said layer of polysilicon of said at least one gate electrode.